

REMARKS

Claims 8, 9, 11-14, and 21 are presently pending and stand rejected. Claims 1-7, 10, and 15-20 are cancelled without prejudice.

Claims 8, 9, 11-14 and 21 were rejected under 35 U.S.C. 112. Assignee has amended the claims and respectfully submits that the foregoing rejection is now overcome.

Claims 8, 9, and 11-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sotheran. Assignee has amended claim 8 recites, among other limitations, “wherein the rasterizing circuit rasterizes the first frame, if the controller does not provide the information regarding the second frame to the display engine before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame”.

Examiner has indicated that “Sotheran explains, ‘The display address generator requests a new display buffer, one every vsync, via a two-wire interface. If there is a buffer flagged as READY, then that will be allocated to display by the buffer manager. If there is no READY buffer, the previously displayed buffer will be repeated’ (see Column 296, Lines 17-21). Therefore, Sotheran teaches not providing the information ... regarding the second frame to the display engine following a vertical synchronization pulse Sotheran also goes on to define ‘vdelay’ as ‘The number of hsync pulse following a vsync pulse before the first line of video of video or border ... The minimum vdelay is zero. The first hsync is the first active line’ (see Column 333, Lines 48-59). Therefore, Sotheran clearly teaches at least one first horizontal synchronization pulse ... following vertical synchronization pulse.”

Assignee respectfully traverses the rejection, because although Sotheran teaches that “display address generator requests a new display buffer, one every vsync”, Sotheran does not indicate when during the vsync such request is made. More particularly, Sotheran does not teach that the foregoing occurs either before or after vsync + vdelay. Thus, Sotheran does not teach “wherein the rasterizing circuit rasterizes the first frame, if the controller does not provide the information regarding the second frame to the display engine **before a first horizontal synchronization pulse** following a vertical synchronization pulse associated with the second frame”.

Accordingly, Assignee respectfully requests that Examiner withdraws the rejection to claims 8 , 9, and 11-15.

Additionally, claim 21 recites, among other limitations, “wherein the rasterizing circuit rasterizes the second frame, if the controller provides the information regarding the second frame to the rasterizing circuit after the vertical synchronization pulse associated with the second frame and before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame.”

Sotheran at col. 295, line 45 – column 296, line 40, clearly does not teach or fairly suggest “wherein the rasterizing circuit *rasterizes the second frame*, if the controller provides the information regarding the second frame to the rasterizing circuit *after the vertical synchronization pulse associated with the second frame* and before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame”. Note that “rasterizes the **second frame**, if the controller provides the information ... *after the vertical synchronization pulse* and before a first horizontal synchronization pulse following a vertical synchronization pulse”, is in contrast with “requests a new display buffer, once very vsync If there is no READY Buffer, the previously displayed buffer will be repeated”.

Accordingly, Assignee respectfully requests allowance of claim 21.

CONCLUSION

For at least the foregoing reasons, each of the pending claims are now in a condition for allowance and Examiner is requested to pass this case to issuance.

The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,



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